S/N 09/256,643 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Michael Trinh
Serial No.:	09/256,643	Group Art Unit:	2822
Filed:	February 23, 1999	Docket:	303.324US2
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

3/4 Supp Prior Art

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

11/25/02

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of $180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

11/19/2002 BABRAHA1 00000025 09256643
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Respectfully submitted,

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By their Representatives,

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Date 13 November 2002 By _____

Robert E. Mates
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 13th day of November, 2002.

Name Amy Moriarty Signature _____